projection electrode may be deformed uniformly. The above discussion is supported in lines 4 - 13, page 10 of the applicants' specification.

Moreover, with respect to the above amendments to page 9 of the applicants' specification, by half-thermosetting the insulating adhesive 38, when the semiconductor chip 31 is mounted on the substrate 37, the semiconductor chip 31 is tentatively strongly adhered to the substrate 37, but a small degree of viscosity of the insulating adhesive 38 is retained for an alignment process.

Accordingly, the withdrawal of the outstanding objections to the specification under 35 USC §112, first paragraph, is in order, and is therefore respectfully solicited.

Moreover, for the same reasons set forth above in the Examiner's outstanding objections to the specification, claims 1 - 8 stand rejected under 35 USC 112, first paragraph. The applicants respectfully request reconsideration of this rejection.

It is submitted that for the reasons set forth above in traversing the outstanding objections to the specification under 35 USC §112, first paragraph, the outstanding rejection of claims 1 - 8 under the same patent statute is in order, and is therefore respectfully solicited.

Furthermore, claims 1 - 8 stand rejected under 35 USC 112, second paragraph, due to certain informalities in the language of claims 1 and 5, which the Examiner deemed needed correction. The applicants respectfully request reconsideration of this rejection.

As indicated above, claims 1 and 5 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention, and in order to correct certain informalities, including those which have been pointed out by the Examiner.

Accordingly, the withdrawal of the outstanding rejection under 35 USC §112, second paragraph, is in order, and is therefore respectfully solicited.

As to the merits of this case, first, claims 1, 2 and 5 - 8 stand rejected under 35 USC 103 based on the applicants' discussion of the prior art[1] in view of Maeda (U.S. Patent No. 4,880,486).

[1] Here, the Examiner specifically relies on line 23, page 1 through line 22, page 2 of the applicants' specification. See, also, the applicants' Figures 1A through 1E.

Secondly, claims 3 and 4 stand rejected under 35 USC 103 based on the above-noted applicants' discussion of the prior art in view of Maeda, and further in view of Fujimoto (U.S. Patent No. 5,115,545). The applicants respectfully request reconsideration of these rejections.

The applicants' claimed invention, as now recited in independent claim 1, is directed to a fabrication method of a semiconductor device including the steps of: (a) forming a plurality of projection electrodes on each of a plurality of semiconductor chips, and applying a thermosetting insulating adhesive to areas of mounting parts where the semiconductor chips are to be mounted on a substrate; (b) heating the thermosetting insulating adhesive on the substrate with a half-thermosetting temperature so as to retain a degree of viscosity of the thermosetting insulating adhesive, and, concurrently, aligning the semiconductor chips to the mounting parts of the substrate, and performing a first fixing of the semiconductor chips with a first pressure; and (c) thereafter heating the substrate, on which the semiconductor chips are fixed, with a thermosetting temperature of the thermosetting insulating adhesive, and performing a second fixing of the semiconductor chips with a second pressure.

Significant features of the applicants' claimed fabrication method, as now set forth in independent claim 1, include the claimed steps of heating the thermosetting insulating adhesive on the substrate with a half-thermosetting temperature so as to retain a degree of viscosity of the thermosetting insulating adhesive, and, concurrently, aligning the semiconductor chips to the mounting parts of the substrate, and performing a first fixing of the semiconductor chips with a first pressure.

The above-discussed significant features of the claimed method, as now set forth in claim 1, are described lines 10 - 18, page 9 of the applicants' specification as follows:

> Then, in the device 25, the semiconductor chip 31 is absorbed by a bonding head 40, and each stud-bump 34 is aligned over a respective mounting pad 37a of the substrate 37. [In the same process], the bonding head 40 with the semiconductor chip 31 is pressed against the mounting pads 37a with the first pressure to perform a tentative fixing (a step S6 in FIG. 3, FIG. 4E). [Concurrently], the insulating adhesive 38 on the substrate 37 is cured by the heat plate 39.

In other words, according to the applicants' instant invention, in the cure/alignment-and-pressing device 25, the heating process of the thermosetting insulating adhesive with a half-thermosetting temperature and the aligning process of the semiconductor chip for the first fixing process are simultaneously performed.

As to the primary reference, the Examiner acknowledges that such primary reference:

> does not teach a process comprising the steps of heating the adhesive on the substrate with a half-thermosetting temperature, and performing a first fixing of the chips with a first pressure in addition to the final fixing step.[2]

Emphasis added.

As to the secondary reference of Maeda ('486), such reference discloses that an adhesive is applied on a substrate, and the adhesive with the substrate is heated to set all the adhesive to be in a half-thermosetting condition. Thereafter, each chip is mounted to the substrate.

However, in the methods disclosed in such reference, after the adhesive is half-thermoset, a mounting process of the chip is carried out. Therefore, in such reference, precise adjustment of the viscosity of the adhesive is required.[3]

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[2] See, lines 18 - 21, page 5 of the outstanding Action.

[3] Similarly, the Akiguchi references disclose that an adhesive is applied on a substrate, and the adhesive with the substrate is heated to set all the adhesive to be in a half-thermosetting condition. Thereafter, each chip is mounted to the substrate.

Furthermore, Maeda (Japanese Laid-Open Patent Application No. 58-180091), cited in the "Notice of References Cited" discloses that before mounting the chip, the adhesive is heated with the half-thermosetting temperature and thereafter, each chip is mounted.

To the contrary, according to applicants' claimed invention, the heating process with the half-thermosetting temperature (referred to as "half-heating process") and the aligning process for the first fixing process (mounting process) are simultaneously carried out in the same process (i.e., at the same time).

That is, in the claimed invention, for each chip, the half-heating process and the aligning process (mounting process) are simultaneously carried out. Therefore, even if the adhesive is substantially hardened by a fast thermosetting process, the chip has been previously aligned and fixed by the first fixing pressure. Accordingly, it is not necessary in the applicants' claimed invention to precisely adjust viscosity of the adhesive.

Furthermore, according to the applicants' claimed invention, in the half-heating and aligning process, the heating process is performed with a half-thermosetting temperature. Therefore, a complex and large equipment is not necessary for the half-heating process.

However, as in Maeda ('486), the above-noted references, after the adhesive is half-thermoset, a mounting process of the chip is carried out. Therefore, in such references, precise adjustment of the viscosity of the adhesive is similarly required.

Maeda ('486) does not suggest, expressed or implied, that the half-heating process of the adhesive and the aligning process of the semiconductor chip are carried out in the same process (at the same time).

In view of the above, even if, arguendo, the teachings of the applicants' discussion of the prior art and Maeda ('486) can be combined in the manner suggested by the Examiner, such combined teachings of such references would still fall far short in fully meeting the applicants' claimed invention, as now recited in claim 1, based on the teachings of the cited prior art references, singly or in combination. Accordingly, a person of ordinary skill in the art would not have found the applicants' claimed invention, as now set forth in claim 1, obvious under 35 USC §103 based on the applicants' discussion of the prior art in view of Maeda ('486).

Also, claims 2 and 5 - 8 depend on claim 1, and further limit the scope of claim 1. Thus, at least for the reasons set forth above with respect to claim 1, claims 2 and 5 - 8 should now be similarly allowable.

In view of the above, the withdrawal of the outstanding rejection under 35 USC §103 based on the applicants' discussion of the prior art[4] in view of Maeda (U.S. Patent No. 4,880,486) is in order, and is therefore respectfully solicited.

As to the other secondary reference of Fujimoto, such Fujimoto reference discloses that after a chip is fixed by original viscosity of an adhesive, a pressing and fixing process is carried out in another process. In other words, the two above processes in Fujimoto are carried out at different times.

To the contrary, according to the applicants' claimed invention, as discussed above, the half-heating process and the aligning process are simultaneously carried out in the same process (at the same time). That is, while the chip is aligned and pressed, the adhesive is half-thermoset. Therefore, at the second fixing of the semiconductor chip with the second pressure, the semiconductor chip is prevented from shifting.

The Fujimoto reference fails to suggest, expressed or implied, that the adhesive is half-thermoset for shift prevention and alignment of the semiconductor chip. Further, in the Fujimoto reference, the thermosetting adhesive is not used.

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[4] Line 23, page 1 through line 22, page 2 of the applicants' specification; and the applicants' Figures 1A through 1E.

In view of the above, it is submitted that even if, arguendo, the teachings of the applicants' discussion of the prior art, Maeda and Fujimoto can be combined in the manner suggested by the Examiner, such combined teachings would still fall far short in fully meeting the applicants' claimed invention, as now recited in independent claim 1 from which claims 3 and 4 depend. Thus, a person of ordinary skill in the art would not have found the applicants' claimed invention, as now recited in independent claim 1 from which claims 3 and 4 depend, obvious under 35 USC §103 based on the applicants' discussion of the prior art (in the applicants' specification), Maeda and Fujimoto, singly or in combination.

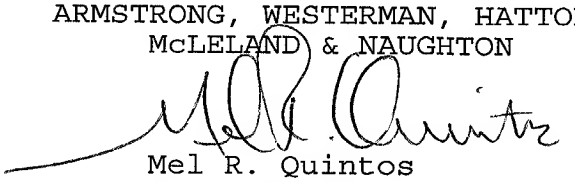
In view of the above, the withdrawal of the outstanding rejection under 35 USC §103 based on the applicants' discussion of the prior art in view of Maeda, and further in view of Fujimoto (U.S. Patent No. 5,115,545) is in order, and is therefore respectfully solicited.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI,
McLELAND & NAUGHTON



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Enclosures: (1) Petition for Extension of Time
(2) Information Disclosure Statement